

INTERNATIONAL STANDARD

ISO/IEC 14776-115

First edition
2004-11

Information technology – Small computer system interface (SCSI) – Part 115: Parallel Interface-5 (SPI-5)

© ISO/IEC 2004

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

ISO/IEC Copyright Office • Case postale 56 • CH-1211 Genève 20 • Switzerland



PRICE CODE **XG**

For price, see current catalogue

Contents

	Page
Foreword	19
Introduction	20
1 Scope	21
2 Normative references	22
2.1 Normative references	22
2.2 Approved references	22
2.3 References under development	23
2.4 Other references	23
3 Definitions, symbols, abbreviations, and conventions	23
3.1 Definitions	23
3.2 Symbols and abbreviations	32
3.3 Keywords	33
3.4 Conventions	34
3.5 Notation for Procedures and Functions	35
4 SCSI parallel interface model	36
4.1 SCSI parallel interface model overview	36
4.2 Cables, connectors, signals, transceivers	36
4.3 Physical architecture of bus segment	36
4.4 Driver-receiver connections	37
4.5 Physical topology details and definitions	37
4.6 Bus segment loading	39
4.7 Termination requirements	39
4.8 SCSI device Addressing	39
4.9 Clocking methods for data transfers	40
4.10 Paced transfer on a SCSI bus	42
4.11 Data transfers	44
4.11.1 Data transfer modes	44
4.11.1.1 Asynchronous transfers	44
4.11.1.2 Synchronous transfers	44
4.11.1.3 Paced transfers	44
4.11.2 ST DATA phase parallel transfers	44
4.11.3 DT DATA phase parallel transfers	45
4.11.3.1 DT DATA phase parallel transfers format	45
4.11.3.2 Data group transfers	45
4.11.3.3 Information unit transfers	45
4.12 Negotiation	46
4.12.1 Negotiation introduction	46
4.12.2 Negotiation algorithm	46
4.12.3 When to negotiate	47
4.12.4 Negotiable fields	48
4.12.4.1 Negotiable fields introduction	48
4.12.4.2 Transfer agreements	49
4.12.4.3 Transfer period factor	49
4.12.4.4 REQ/ACK offset	51
4.12.4.5 Transfer width exponent	52
4.12.4.6 Protocol options	52
4.12.4.6.1 Protocol options introduction	52
4.12.4.6.2 IU_REQ	53
4.12.4.6.3 DT_REQ	54

4.12.4.6.4 QAS_REQ	54
4.12.4.6.5 HOLD_MCS	54
4.12.4.6.6 WR_FLOW	55
4.12.4.6.7 RD_STRM	55
4.12.4.6.8 RTI	55
4.12.4.6.9 PCOMP_EN	55
4.12.5 Negotiable field combinations	56
4.12.6 Message restrictions	57
4.12.7 Negotiation message sequences	58
4.12.7.1 Negotiation message sequences overview	58
4.12.7.2 SCSI initiator port originated PPR negotiation	59
4.12.7.3 SCSI initiator port originated WDTR negotiation	60
4.12.7.4 SCSI initiator port originated SDTR negotiation	62
4.12.7.5 SCSI target port originated WDTR negotiation	64
4.12.7.6 SCSI target port originated SDTR negotiation	67
4.13 Protocol	68
5 SCSI parallel interface connectors	71
5.1 SCSI parallel interface connectors overview	71
5.2 Non-shielded connector	71
5.2.1 Non-shielded connector alternative 1 - A cable	71
5.2.2 Non-shielded connector alternative 2 - A cable	71
5.2.3 Non-shielded connector alternative 3 - P cable	72
5.2.4 Non-shielded connector alternative 4	72
5.3 Shielded connector	78
5.3.1 Shielded connector overview	78
5.3.2 Shielded connector alternative 1 - A cable	78
5.3.3 Shielded connector alternative 2 - A cable	78
5.3.4 Shielded connector alternative 3 - P cable	78
5.3.5 Shielded connector alternative 4 - P cable	78
5.4 Connector contact assignments	86
5.4.1 Connector contact assignments overview	86
5.4.2 Differential connector contact assignments	87
6 SCSI bus segment interconnect	90
6.1 SCSI bus segment interconnect overview	90
6.2 SCSI bus segment cables	90
6.3 Interconnect characteristics for signals	91
6.3.1 SCSI bulk cable	91
6.3.2 Minimum conductor size for signals	92
6.3.3 Local transmission line impedance	92
6.3.4 Extended distance transmission line impedance	92
6.3.5 Capacitance	92
6.3.6 Differential propagation time and propagation time skew	92
6.3.7 Differential attenuation	92
6.3.8 Crosstalk	93
6.4 Decoupling characteristics for TERMPWR lines	93
6.5 Connection requirements for RESERVED lines	94
6.6 Cables used with LVD transceivers	94
6.7 LVD stub length and spacing	95
7 SCSI parallel interface electrical characteristics	96
7.1 SCSI parallel interface electrical characteristics overview	96
7.2 LVD termination	96
7.2.1 LVD termination overview	96
7.2.2 LVD driver characteristics	101
7.2.3 LVD receiver characteristics	104

7.2.4 LVD capacitive loads	105
7.2.4.1 Management of LVD release glitches	107
7.2.5 SE/HVD transmission mode detection	109
7.2.5.1 SE/HVD transmission mode detection overview	109
7.2.5.2 LVD DIFFSENS driver	109
7.2.5.3 LVD DIFFSENS receiver	110
7.3 Terminator power	112
8 SCSI bus signals	114
8.1 SCSI bus signals overview	114
8.2 Signal descriptions	114
8.3 LVD Signal states	117
8.4 OR-tied signals	118
8.5 Signal sources	118
9 SCSI parallel bus timing	120
9.1 SCSI parallel bus timing values	120
9.2 Timing description	126
9.2.1 Arbitration delay	126
9.2.2 ATN transmit setup time	127
9.2.3 ATN receive setup time	127
9.2.4 Bus clear delay	127
9.2.5 Bus free delay	127
9.2.6 Bus set delay	127
9.2.7 Bus settle delay	128
9.2.8 Cable skew	128
9.2.9 Chip noise in receiver	128
9.2.10 Clock jitter	128
9.2.11 Crosstalk time shift	128
9.2.12 Flow control receive hold time	128
9.2.13 Flow control receive setup time	128
9.2.14 Flow control transmit hold time	128
9.2.15 Flow control transmit setup time	128
9.2.16 Offset induced time asymmetry	129
9.2.17 pCRC receive hold time	129
9.2.18 pCRC receive setup time	129
9.2.19 pCRC transmit hold time	129
9.2.20 pCRC transmit setup time	129
9.2.21 Data release delay	129
9.2.22 DIFFSENS voltage filter time	129
9.2.23 Physical disconnection delay	129
9.2.24 Power on to selection	129
9.2.25 QAS arbitration delay	130
9.2.26 QAS assertion delay	130
9.2.27 QAS release delay	130
9.2.28 QAS non-DATA phase REQ(ACK) period	130
9.2.29 Receive assertion period	130
9.2.30 Receive hold time	130
9.2.31 Receive internal hold time	130
9.2.32 Receive internal setup time	130
9.2.33 Receive negation period	131
9.2.34 Receive setup time	131
9.2.35 Receive REQ(ACK) period tolerance	131
9.2.36 Receive REQ assertion period with P_CRCA transitioning	131
9.2.37 Receive REQ negation period with P_CRCA transitioning	131
9.2.38 Receive Skew Compensation	131
9.2.39 Receiver amplitude time skew	131

9.2.40 Receiver de-skewed data valid window	131
9.2.41 REQ(ACK) period	132
9.2.42 Reset delay	132
9.2.43 Reset hold time	132
9.2.44 Reset to selection	132
9.2.45 Residual skew error	133
9.2.46 Selection abort time	133
9.2.47 Selection time-out delay	133
9.2.48 Signal timing skew	133
9.2.49 Skew correction range	133
9.2.50 Strobe offset tolerance	134
9.2.51 System deskew delay	134
9.2.52 System noise at launch	134
9.2.53 System noise at receiver	134
9.2.54 Time asymmetry	134
9.2.55 Transmit assertion period	134
9.2.56 Transmit hold time	135
9.2.57 Transmit ISI Compensation	135
9.2.58 Transmit negation period	135
9.2.59 Transmit setup time	135
9.2.60 Transmit REQ(ACK) period tolerance	135
9.2.61 Transmit REQ assertion period with P_CRCA transitioning	135
9.2.62 Transmit REQ negation period with P_CRCA transitioning	135
9.2.63 Transmitter skew	135
9.2.64 Transmitter time asymmetry	136
9.3 Measurement points	136
9.3.1 Measurement points overview	136
9.3.2 LVD measurement points	137
9.4 Receiver Masks	139
9.4.1 Synchronous transfers and for fast-160 paced transfer clocking signals	139
9.4.2 Paced transfers with precompensation enabled on fast-160	140
9.4.3 Paced transfers with precompensation disabled on fast-160 and fast-320	142
9.5 Timing parameters	148
9.6 Setup and hold timings	148
9.6.1 ST data transfer calculations	148
9.6.2 DT data transfer calculations	149
10 SCSI bus phases	151
10.1 SCSI bus phases overview	151
10.2 BUS FREE phase	151
10.3 Expected and unexpected bus free phases	151
10.4 Arbitration	152
10.4.1 Arbitration and QAS overview	152
10.4.2 NORMAL ARBITRATION phase	152
10.4.3 QAS protocol	153
10.4.4 QAS phase	154
10.5 SELECTION phase	155
10.5.1 Selection Overview	155
10.5.2 Selection using attention condition	156
10.5.2.1 Starting the SELECTION phase when using attention condition	156
10.5.2.2 Information unit transfers disabled	156
10.5.2.3 Information unit transfers enabled	156
10.5.2.4 Selection using attention condition time-out procedure	156
10.5.3 Selection without using attention condition	157
10.5.3.1 Information unit transfers disabled or enabled	157
10.5.3.2 Selection without using attention condition time-out procedure	157
10.6 RESELECTION phase	158

10.6.1 RESELECTION phase overview	158
10.6.2 Physical reconnection	158
10.6.3 Physical reconnection time-out procedure	159
10.7 Information transfer phases	159
10.7.1 Information transfer phases overview	159
10.7.2 Asynchronous transfer	160
10.7.3 Synchronous transfer	161
10.7.3.1 Synchronous transfer overview	161
10.7.3.2 ST synchronous transfer	161
10.7.3.3 DT synchronous transfer	162
10.7.3.3.1 DT synchronous transfer overview	162
10.7.3.3.2 Information unit transfer	162
10.7.3.3.3 DT DATA IN phase information unit transfer exception condition handling	163
10.7.3.3.4 DT DATA OUT phase information unit transfer exception condition handling	164
10.7.3.3.5 Data group data field transfer	165
10.7.3.3.6 Data Group Pad field and pCRC field transfer to SCSI initiator port	165
10.7.3.3.7 Data Group Pad field and pCRC field transfer to SCSI target port	167
10.7.4 Paced transfer	168
10.7.4.1 Paced transfer overview	168
10.7.4.2 Paced transfer training pattern	169
10.7.4.2.1 Training pattern overview	169
10.7.4.2.2 DT DATA IN phase training pattern	170
10.7.4.2.3 DT DATA OUT phase training pattern	171
10.7.4.3 P1 data valid/invalid state transitions	172
10.7.4.3.1 P1 data valid/invalid state transitions overview	172
10.7.4.3.2 Starting pacing transfers at end of training pattern	173
10.7.4.3.3 Starting pacing transfers with no training pattern	173
10.7.4.3.4 Ending pacing transfers	174
10.7.4.4 Paced information unit transfer	174
10.7.4.5 Deskewing	175
10.7.5 Wide transfer	175
10.8 COMMAND phase	176
10.8.1 COMMAND phase description	176
10.8.2 COMMAND phase exception condition handling	176
10.9 DATA phase	177
10.9.1 DATA phase overview	177
10.9.2 DT DATA IN phase	177
10.9.3 DT DATA OUT phase	177
10.9.4 ST DATA IN phase	177
10.9.5 ST DATA OUT phase	177
10.10 STATUS phase	177
10.10.1 STATUS phase description	177
10.10.2 STATUS phase exception condition handling	178
10.11 MESSAGE phase	178
10.11.1 MESSAGE phase overview	178
10.11.2 MESSAGE IN phase	178
10.11.3 MESSAGE IN phase exception condition handling	178
10.11.4 MESSAGE OUT phase	178
10.11.5 MESSAGE OUT phase exception condition handling	179
10.12 Signal restrictions between phases	179
11 DATA BUS protection	181
11.1 DATA BUS protection overview	181
11.2 ST DATA BUS protection using parity	181
11.3 DT DATA BUS protection using CRC	181
11.3.1 DT DATA BUS protection using CRC overview	181
11.3.2 Error detection capabilities	181

11.3.3 Order of bytes in the CRC field	182
11.3.4 CRC generation and checking	184
11.3.5 Test cases	184
12 SCSI bus conditions	185
12.1 SCSI bus conditions overview	185
12.2 Attention condition	185
12.3 Bus reset condition	186
12.4 Hard reset	186
12.5 Reset events	187
12.5.1 Reset events overview	187
12.5.2 Bus reset event	187
12.5.3 Power on reset event	187
12.5.4 Target reset event	187
13 SCSI bus phase sequences	188
13.1 SCSI bus phase sequences overview	188
13.2 Phase sequences with information units disabled	189
13.2.1 Phase sequences for physical reconnection or selection using attention condition	189
13.2.2 Phase sequences for selection without using attention condition	190
13.3 Phase sequences with information unit enabled	191
13.3.1 Phase sequences for physical reconnection or selection without using attention condition ..	191
13.3.2 Phase sequences for selection using attention condition	192
14 SPI information units	193
14.1 SPI information unit overview	193
14.2 Information unit transfer logical operations	193
14.3 SPI information units	199
14.3.1 SPI command information unit	199
14.3.2 SPI L_Q information unit	203
14.3.3 SPI data information unit	206
14.3.4 SPI data stream information unit	207
14.3.5 SPI status information unit	208
15 SCSI pointers	212
16 SCSI messages	213
16.1 SCSI messages overview	213
16.2 Message protocols and formats	213
16.2.1 Message protocol rules	213
16.2.2 Message formats	213
16.2.3 One-byte messages	214
16.2.4 Two-byte messages	214
16.2.5 Extended messages	214
16.3 Link control messages	216
16.3.1 Link control message codes	216
16.3.2 DISCONNECT	217
16.3.3 IDENTIFY	217
16.3.4 IGNORE WIDE RESIDUE	218
16.3.5 INITIATOR DETECTED ERROR	219
16.3.6 LINKED COMMAND COMPLETE	219
16.3.7 MESSAGE PARITY ERROR	219
16.3.8 MESSAGE REJECT	219
16.3.9 MODIFY DATA POINTER	220
16.3.10 MODIFY BIDIRECTIONAL DATA POINTER	221
16.3.11 NO OPERATION	222
16.3.12 PARALLEL PROTOCOL REQUEST	222

16.3.13 QAS REQUEST	222
16.3.14 RESTORE POINTERS	223
16.3.15 SAVE DATA POINTERS	223
16.3.16 SYNCHRONOUS DATA TRANSFER REQUEST	223
16.3.17 TASK COMPLETE	223
16.3.18 WIDE DATA TRANSFER REQUEST	224
16.4 Task attribute messages	224
16.4.1 Task attribute message overview and codes	224
16.4.2 ACA	225
16.4.3 HEAD OF QUEUE	226
16.4.4 ORDERED	226
16.4.5 SIMPLE	227
16.5 Task management messages	228
16.5.1 Task management message codes	228
16.5.2 ABORT TASK	228
16.5.3 ABORT TASK SET	229
16.5.4 CLEAR ACA	229
16.5.5 CLEAR TASK SET	229
16.5.6 LOGICAL UNIT RESET	229
16.5.7 TARGET RESET	230
17 Command processing considerations and exception conditions	231
17.1 Command processing considerations and exception conditions overview	231
17.2 Asynchronous event notification	231
17.3 Incorrect initiator connection	231
17.4 Unexpected RESELECTION phase	232
18 SCSI management features for the SCSI parallel interface	233
18.1 SCSI mode parameters	233
18.1.1 SCSI mode parameter overview and codes	233
18.1.2 Disconnect-Reconnect mode page	234
18.1.3 Logical Unit Control mode page	237
18.1.4 Port Control mode page	238
18.1.4.1 Port Control mode page overview	238
18.1.4.2 Margin Control mode subpage	240
18.1.4.3 Saved Training Configuration Values mode subpage	242
18.1.4.4 Negotiated Settings mode subpage	244
18.1.4.5 Report Transfer Capabilities mode subpage	245
19 SCSI parallel interface services	246
19.1 SCSI parallel interface services overview	246
19.2 Procedure objects	246
19.3 Application client SCSI command services	247
19.3.1 Application client SCSI command services overview	247
19.3.2 Send SCSI command service	248
19.4 Device server SCSI command services	248
19.4.1 Device server SCSI command services overview	248
19.4.2 Data-in delivery service	248
19.4.3 Data-out delivery service	249
19.5 Task management services	249
19.5.1 Task management functions overview	249
19.5.2 Task management functions	249
19.5.3 ABORT TASK	250
19.5.4 ABORT TASK SET	250
19.5.5 CLEAR ACA	250
19.5.6 CLEAR TASK SET	250
19.5.7 LOGICAL UNIT RESET	250

19.5.8 RESET SERVICE DELIVERY SUBSYSTEM	250
19.5.9 TARGET RESET	250
19.5.10 WAKEUP	250
Annex A (normative) Additional requirements for LVD SCSI drivers and receivers	251
A.1 System level requirements	251
A.2 Driver requirements	253
A.2.1 Driver requirements overview	253
A.2.2 Differential output voltage, V_S	253
A.2.3 Offset (common-mode output) voltage (V_{CM})	257
A.2.4 Short-circuit currents (I_{O-S} and I_{O+S})	258
A.2.5 Open-circuit output voltages ($V_{O-(OC)}$ and $V_{O+(OC)}$)	259
A.2.6 Output signal waveform	260
A.2.7 Dynamic output signal balance ($V_{CM(PP)}$)	261
A.3 Receiver characteristics	263
A.3.1 Receiver characteristics overview	263
A.3.2 Receiver steady state input voltage requirements	263
A.3.2.1 Steady state input voltage requirements for fast-160 and slower receivers	263
A.3.2.2 Steady state input voltage requirements for fast-320 receivers	263
A.3.3 Compliance test	264
A.3.4 Receiver setup and hold times	265
A.3.5 Fast-160 receiver bandwidth specifications	265
A.4 Transceiver characteristics	267
A.4.1 Transceiver output/input currents, I_{I-L} and I_{I+L}	267
A.4.2 Transceiver maximum input voltages	267
Annex B (normative) SCSI bus fairness	268
B.1 Model	268
B.2 Determining fairness by monitoring prior bus activity	268
B.2.1 Fairness for normal arbitration method	268
B.2.2 Fairness for QAS	269
B.3 Fairness algorithm	269
B.3.1 Fairness states overview	269
B.3.2 Fairness idle state	269
B.3.3 Fairness wait state	269
B.3.4 Fairness participate state	269
B.3.5 Lockout delay	269
B.3.6 Mixed arbitration	270
B.4 SCSI initiator port fairness recommendations	270
Annex C (normative) Non-shielded connector alternative 4	271
C.1 Non-shielded connector alternative 4 signal definitions	271
C.2 VOLTAGE and GROUND signals	271
C.3 CHARGE signals	272
C.4 SPINDLE SYNC	272
C.5 ACTIVE LED OUT	273
C.6 Motor start controls	273
C.7 SCSI ID selection	274
C.8 MATED signals	275
C.8.1 MATED signals overview	275
C.8.2 MATED 2/drive side	276
C.8.3 MATED 2/backplane side	276
C.8.4 MATED 1/drive side	276
C.8.5 MATED 1/backplane side	276

Annex D (normative) Removal and insertion of SCSI devices	278
D.1 Removal and insertion of SCSI devices overview	278
D.2 Case 1 - Power off during removal or insertion	278
D.3 Case 2 - RST signal asserted continuously during removal or insertion	278
D.4 Case 3 - Current I/O processes not allowed during insertion or removal	278
D.5 Case 4 - Current I/O process allowed during insertion or removal	279
Annex E (normative) Simple expander requirements	280
E.1 Introduction	280
E.2 Glossary	280
E.3 Bus segments in a SCSI domain	280
E.4 Simple bus expanders	281
E.5 Homogeneous type	282
E.6 Heterogeneous types	282
E.7 SCSI domain examples using simple expanders	282
E.8 Rules for SCSI domains using simple expanders	283
E.8.1 Rule summary	283
E.8.2 Rule 1	284
E.8.3 Rule 2	284
E.8.4 Rule 3	285
E.8.5 Rule 4	286
E.8.5.1 Effects of wired-or glitches	286
E.8.5.2 Simple expander propagation delay effects	286
E.8.5.3 Sample calculations	287
E.8.6 Rule 5	288
E.8.7 Rule 6	288
E.9 Special performance considerations for SCSI domains with simple expanders	289
Annex F (normative) Expander Communication Protocol	292
F.1 Introduction	292
F.2 Glossary and Definitions	292
F.3 Symbols and abbreviations	293
F.4 Enabling ECP	293
F.5 Communicative expander function structures	293
F.6 Expander functions	296
F.6.1 Outbound multiple functions	296
F.6.1.1 Outbound multiple function data transfer rules	296
F.6.1.2 ASSIGN ADDRESS	296
F.6.1.3 MARGIN CONTROL	297
F.6.2 Outbound single functions	298
F.6.2.1 Outbound single function data transfer rules	298
F.6.2.2 CONTROL	299
F.6.3 Inbound multiple functions	300
F.6.3.1 Inbound multiple function data transfer rules	300
F.6.3.2 MARGIN REPORT	300
F.6.3.3 REPORT CAPABILITES	301
F.6.3.4 REPORT CURRENT STATUS	302
F.6.4 Inbound single functions	303
F.6.4.1 Inbound single function data transfer rules	303
F.6.4.2 EXPANDER INQUIRY	304
F.6.4.3 REPORT SAVED TRAINING CONFIGURATION VALUES	305
F.7 Data Transfer Requirements	307
Annex G (informative) Interconnecting bus segments of different widths	308

Annex H (informative) SCSI ICONS	310
Annex I (informative) Backplane construction guidelines	311
I.1 Universal backplane construction	311
I.1.1 Universal backplane construction overview	311
I.1.2 Microstrip	311
I.1.3 Embedded Microstrip	311
I.1.4 Stripline	312
I.1.5 Dual Stripline	313
I.1.6 Differential Impedance	314
I.1.7 Single ended impedance	315
I.1.8 Differential stripline	315
I.1.9 Dielectric material selection	318
I.1.10 Vias	318
I.1.11 Transmission Lines	320
Annex J (informative) SPI-5 to SCSI-2 terminology mapping	325
Annex K (informative) Bibliography	326

Tables

	Page
1 LVD transceiver/speed support map	36
2 Negotiable fields and effects of successful negotiation	48
3 Responding message requirements	49
4 Transfer agreements	49
5 Transfer Period Factor	50
6 Transfer Period Factor relationships	51
7 REQ/ACK offset	52
8 Transfer Width Exponent	52
9 Protocol option bits	53
10 Bus phases resulting from iu_req changes	54
11 Valid negotiable field combinations	57
12 Cross-reference to A cable contact assignments	86
13 LVD contact assignments - A cable	87
14 LVD contact assignments - P cable	88
15 LVD contact assignments - non-shielded alternative 4 connector	89
16 LVD local transmission line impedance	92
17 Bulk cable capacitance limits	92
18 Attenuation requirements for SCSI bulk cable	93
19 LVD maximum bus segment path length between terminators	95
20 Minimum stub connection spacing for LVD SCSI devices	95
21 Absolute electrical limits at the device connector	96
22 Input current requirements at the device connector for lines not being driven by the device	96
23 I-V requirements for differential impedance, common mode impedance, and V_{BIAS} tests	99
24 Values for LVD termination balance test	101
25 Fast-160 precompensation	102
26 Values for LVD capacitive loads	107
27 Glitch management requirements for SCSI devices using LVD drivers	108
28 LVD DIFFSENS driver specifications	109
29 DIFFSENS receiver operating requirements	111
30 Terminator power characteristics at the terminator	113
31 Arbitration priorities by SCSI ID	114
32 P_CRC signal usage requirements	116
33 Signal sources	119
34 SCSI bus control timing values	120
35 SCSI bus data & information phase ST timing values	121
36 Miscellaneous SCSI bus data & information phase DT timing values	122
37 Transmit SCSI bus data & information phase DT timing values	123
38 Receive SCSI bus data & information phase DT timing values	124
39 SCSI fast-160 and fast-320 non-compensatable timing budget	125
40 SCSI fast-160 and fast-320 interconnect timing budget	126
41 Receiver Eye Mask Values	143
42 Information transfer phases	160
43 Wide SCSI byte order	176
44 Parity checking rules for SELECTION and RESELECTION phases	181
45 SPI information units	193
46 SPI command information unit	200
47 TASK ATTRIBUTE	201
48 TASK MANAGEMENT FUNCTIONS	202
49 SPI L_Q information unit	204
50 TYPE	205
51 BIDI DIRECTION	206
52 SPI data information unit	207
53 SPI data stream information unit	208
54 SPI status information unit	209
55 PACKETIZED FAILURES field	210

56	PACKETIZED FAILURE CODE	211
57	Message format	214
58	Extended message format	215
59	Extended message codes	215
60	Link control message codes	216
61	IDENTIFY message format	217
62	IGNORE WIDE RESIDUE message format	218
63	IGNORE field definition	219
64	MODIFY DATA POINTER message format	220
65	MODIFY BIDIRECTIONAL DATA POINTER message format	221
66	PARALLEL PROTOCOL message format	222
67	SYNCHRONOUS DATA TRANSFER message format	223
68	WIDE DATA TRANSFER message format	224
69	Task attribute message codes	225
70	ACA message format	226
71	HEAD OF QUEUE message format	226
72	ORDERED message format	226
73	SIMPLE message format	227
74	Task management message codes	228
75	Mode page codes for the SCSI parallel interface	233
76	Mode subpage codes for the SCSI parallel interface	233
77	Disconnect-Reconnect mode page	235
78	DTDC	237
79	Logical Unit Control mode page	238
80	Port Control mode page short format	239
81	Port Control mode subpage format	240
82	Margin Control mode subpage	241
83	Summary of margin control field values	242
84	Saved Training Configuration mode subpage	243
85	Negotiated Settings mode subpage	244
86	Bus mode	245
87	Report Transfer Capabilities mode subpage	245
88	This standards objects mapped to objects from other SCSI standards	246
89	Procedure objects	247
90	Processing of send SCSI command service procedure	248
91	Processing of data-in delivery service procedure	249
92	Processing of data-out delivery service procedure	249
A.1	System level requirements	252
A.2	Driver steady-state test limits and conditions for non-paced transfers	254
A.3	Driver steady-state test limits and conditions for paced transfers	254
A.4	Driver switching test circuit parameters	261
A.5	Dynamic output balance limits	262
A.6	Receiver steady state input voltage ranges	263
A.7	Fast-320 receiver steady state input voltage ranges	264
A.8	Receiver minimum and maximum input voltages	265
A.9	Properties of receiver pulse train	266
C.1	Voltage specification limits	271
C.2	Charge supply to SCSI device	272
C.3	Output characteristics of drive ACTIVE LED OUT signal	273
C.4	Definition of motor start controls	274
C.5	Electronic requirements for input controls	274
C.6	SCSI device ID selection signals	275
E.1	SCSI Domain rules	284
E.2	SCSI domain delay calculation	288
E.3	Minimum REQ/ACK OFFSET for maximum performance	291
F.1	Expander function header	294
F.2	Expander functions	295

F.3 SEDB format	295
F.4 Device class	296
F.5 ASSIGN ADDRESS SEDB	297
F.6 MARGIN CONTROL SEDB	298
F.7 CONTROL data structure	299
F.8 FAR_CTL field values	300
F.9 MARGIN REPORT SEDB	301
F.10 REPORT CAPABILITES SEDB	302
F.11 REPORT CURRENT STATUS SEDB	303
F.12 EXPANDER INQUIRY expander function header	304
F.13 EXPANDER INQUIRY data	305
F.14 REPORT SAVED TRAINING CONFIGURATION VALUES data structure	306
I.1 Dielectric constants	318
J.1 SPI-5 to SCSI-2 terminology mapping	325

Figures

	Page
1 SCSI Document Structure	22
2 Differential SCSI bus segment	37
3 SCSI bus segment topology details	38
4 ST latching data vs. DT latching data	40
5 ST synchronous transfer example	41
6 DT synchronous transfer example	41
7 Paced transfer example	42
8 Example of a SCSI bus with fast-160 paced transfers	43
9 Example of a SCSI bus with fast-320 paced transfers	43
10 Skew compensation and clock shift example	44
11 Error-free negotiation message sequences.	47
12 SCSI initiator port originated PPR negotiation: SCSI initiator port response	59
13 SCSI initiator port originated PPR negotiation: SCSI target port response	60
14 SCSI initiator port originated WDTR negotiation: SCSI initiator port response	61
15 SCSI initiator port originated WDTR negotiation: SCSI target port response	62
16 SCSI initiator port originated SDTR negotiation: SCSI initiator port response	63
17 SCSI initiator port originated SDTR negotiation: SCSI target port response	64
18 SCSI target port originated WDTR negotiation: SCSI target port response	65
19 SCSI target port originated WDTR negotiation: SCSI initiator port response	66
20 SCSI target port originated SDTR negotiation: SCSI target port response	67
21 SCSI target port originated SDTR negotiation: SCSI initiator port response	68
22 SCSI Parallel Interface service reference mode	69
23 Model for a four step confirmed service	69
24 Model for a two step confirmed service	70
25 50/68-contact alternative 1/alternative 3 non-shielded SCSI device connector	73
26 50/68-contact alternative 1/alternative 3 non-shielded mating connector	74
27 50-contact alternative 2 non-shielded SCSI device connector (A cable)	75
28 50-contact alternative 2 non-shielded mating connector (A cable)	76
29 80-contact alternative 4 non-shielded SCSI device connector (P cable)	77
30 80-contact alternative 4 non-shielded contact positions (P cable)	77
31 50-contact alternative 1 shielded SCSI device connector (A cable)	79
32 50-contact alternative 1 shielded mating connector (A cable)	80
33 50-contact alternative 2 shielded SCSI device connector (A cable)	81
34 50-contact alternative 2 shielded mating connector (A cable)	82
35 68-contact alternative 3 shielded SCSI device connector (P cable)	83
36 68-contact alternative 3 shielded mating connector (P cable)	84
37 68-contact alternative 4 shielded SCSI device connector (P cable)	85
38 68-contact alternative 4 shielded contact positions (P cable)	86
39 Terminator decoupling example	94
40 LVD bus segment terminator	97
41 Test circuit for terminator differential impedance	97
42 Termination I-V characteristics for differential and common mode impedance tests	98
43 Test circuit for termination common mode impedance test	98
44 Termination balance test configuration	100
45 Termination balance test data definition	100
46 Examples of fast-160 driver precompensation	103
47 LVD transceiver architecture	104
48 LVD receiver example	105
49 LVD Capacitive loads	106
50 LVD DIFFSENS driver signal definitions	110
51 DIFFSENS receiver function	110
52 LVD DIFFSENS receiver example	112
53 Voltage and current definitions	117
54 LVD Signaling sense	118
55 Timing budget item locations	126

56 Receiver de-skew parameters	132
57 Skew correction range	134
58 Transmitter skew	136
59 Transmitter time asymmetry	136
60 LVD timing measurement points for ST synchronous transfers	137
61 LVD timing measurement points for DT synchronous transfers	138
62 LVD timing measurement points for DT paced transfers	139
63 LVD receiver mask for synchronous transfers and for fast-160 paced transfer clocking signals	140
64 Fast-160 LVD receiver mask 1 for paced transfers with precompensation enabled	141
65 Fast-160 LVD receiver mask 2 for paced transfers with precompensation enabled	142
66 LVD paced transfer receiver mask non-precompensated signals transitioning at the negotiated transfer period	144
67 LVD paced transfer receiver mask non-precompensated minimum amplitude change	145
68 LVD paced transfer receiver mask non-precompensated non-clocking isolated assertion pulse	146
69 LVD paced transfer receiver mask non-precompensated non-clocking isolated negation pulse	147
70 LVD paced transfer eye mask non-precompensated non-clocking pulse	148
71 System setup and hold timings for ST data transfers	149
72 System setup and hold timings for DT synchronous transfers	150
73 Usage of P1 to establish data valid and data invalid states	173
74 CRC generation and transmission	183
75 Phase sequences for physical reconnection or selection using attention condition with information unit transfers disabled	189
76 Phase sequences for selection without using attention condition with information unit transfers disabled	190
77 Phase sequences for physical reconnection or selection without using attention condition with information unit transfers enabled	191
78 Phase sequences for selection with attention condition with information unit transfers enabled	192
79 SPI information unit sequence during initial connection	195
80 SPI information unit sequence during data type transfers	196
81 SPI information unit sequence during data stream type transfers	197
82 SPI information unit sequence during status transfers	198
A.1 Differential steady-state output voltage test circuit	255
A.2 Domain for driver assertion and negation levels for non-paced transfers	256
A.3 Domain for driver assertion and negation levels for paced transfers	257
A.4 Driver offset steady-state voltage test circuit	258
A.5 Common mode output voltage test	258
A.6 Driver short-circuit test circuit	259
A.7 Open-circuit output voltage test circuit	259
A.8 Differential output switching voltage test circuit	260
A.9 Driver output signal waveform	261
A.10 Driver offset switching voltage test circuit	262
A.11 Input signal offset component ($V_{RXOFFSET}$)	264
A.12 Receiver input voltage threshold test circuit	265
A.13 Fast-160 receiver pulse train example	266
A.14 Transceiver off-state output current test circuit	267
C.1 Sample circuit for mated indications	277
E.1 A two segment domain using a single simple expander circuit	281
E.2 Three ways to couple bus segments together with simple expanders	282
E.3 Examples of SCSI domains using simple expanders	283
E.4 Intermediate bus segments and performance ranking	285
E.5 Two configurations for SCSI domain delay calculations	287
E.6 Examples of illegal loops	289
G.1 Interconnecting LVD A and P cables	309
H.1 LVD icon for SCSI	310
I.1 Microstrip geometry	311
I.2 Embedded microstrip geometry	312
I.3 Stripline geometry	312

I.4 Dual stripline geometry	313
I.5 Lossless model for differential impedance	314
I.6 Edge coupled differential microstrip	316
I.7 Edge coupled differential stripline	316
I.8 Broadside coupled differential stripline	316
I.9 Typical transmission line element	320

**INFORMATION TECHNOLOGY –
SMALL COMPUTER SYSTEM INTERFACE (SCSI) –
PART 115: Parallel interface-5 (SPI-5)**

FOREWORD

- 1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.
- 2) In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.
- 3) All users should ensure that they have the latest edition of this publication.
- 4) No liability shall attach to IEC or ISO or its directors, employees, servants or agents including individual experts and members of their technical committees and IEC or ISO member bodies for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication of, use of, or reliance upon, this ISO/IEC publication or any other IEC, ISO or ISO/IEC publications.
- 5) Attention is drawn to the normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

CAUTION: The developers of this standard have requested that holders of patents that may be required for the implementation of the standard, disclose such patents to the publisher. However, neither the developers nor the publisher have undertaken a patent search in order to identify which, if any, patents may apply to this standard. As of the date of publication of this standard, following calls for the identification of patents that may be required for the implementation of the standard, no such claims have been made. No further patent search is conducted by the developer or the publisher in respect to any standard it processes. No representation is made or implied that licenses are not required to avoid infringement in the use of this standard.

International Standard ISO/IEC 14776-115 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

INTRODUCTION

ISO/IEC 14776-115 defines mechanical, electrical, timing requirements, command sets, and the task management delivery protocol requirements to transfer commands and data between SCSI devices attached to an SCSI parallel interface. The resulting interface facilitates the interconnection of computers and intelligent peripherals and thus provides a common interface standard for both system integrators and suppliers of intelligent peripherals.

INFORMATION TECHNOLOGY - SMALL COMPUTER SYSTEM INTERFACE (SCSI) –

Part 115: Parallel Interface-5 (SPI-5)

1 Scope

This part of ISO/IEC 14776 defines the mechanical, electrical, timing, and protocol requirements of the SCSI parallel interface to allow conforming SCSI devices to inter-operate. The SCSI parallel interface is a local I/O bus that may be operated over a wide range of transfer rates. The objectives of the SCSI parallel interface are:

- a) To provide host computers with device independence within a class of devices. Thus, different disk drives, tape drives, printers, optical media drives, and other SCSI devices may be added to the host computers without requiring modifications to generic system hardware. Provision is made for the addition of special features and functions through the use of vendor-specific options. Reserved areas are provided for future standardization.
- b) To provide compatibility such that conforming SPI-2, SPI-3 devices may interoperate with SPI-5 devices given that the systems engineering is correctly done. Conforming SPI-2, SPI-3, and SPI-5 devices should respond in an acceptable manner to reject SPI-5 protocol extensions. SPI-5 protocol extensions are designed to be permissive of such rejections and thus allow SPI-2 and SPI-3 devices to continue operation without requiring the use of the extensions.

The interface protocol includes provision for the connection of multiple SCSI initiator ports (i.e., SCSI devices capable of initiating an I/O process) and multiple SCSI target ports (i.e., SCSI devices capable of responding to a request to perform an I/O process). Distributed arbitration (i.e., bus-contention logic) is built into the architecture of this standard. A default priority system awards interface control to the highest priority SCSI device that is contending for use of the bus and an optional fairness algorithm is defined.

This standard defines the physical attributes of an input/output bus for interconnecting computers and peripheral devices.

The set of SCSI standards specifies the interfaces, functions, and operations necessary to ensure interoperability between conforming SCSI implementations. This standard is a functional description. Conforming implementations may employ any design technique that does not violate interoperability.

This standard has made obsolete single-ended and multimode signaling alternatives. Implementations that use single-ended or multimode signaling alternatives should reference the SCSI Parallel Interface-2 standard (ISO/IEC 14776-112).

Figure 1 is intended to show the general structure of SCSI standards. The figure is not intended to imply a relationship such as a hierarchy, protocol stack, or system architecture.

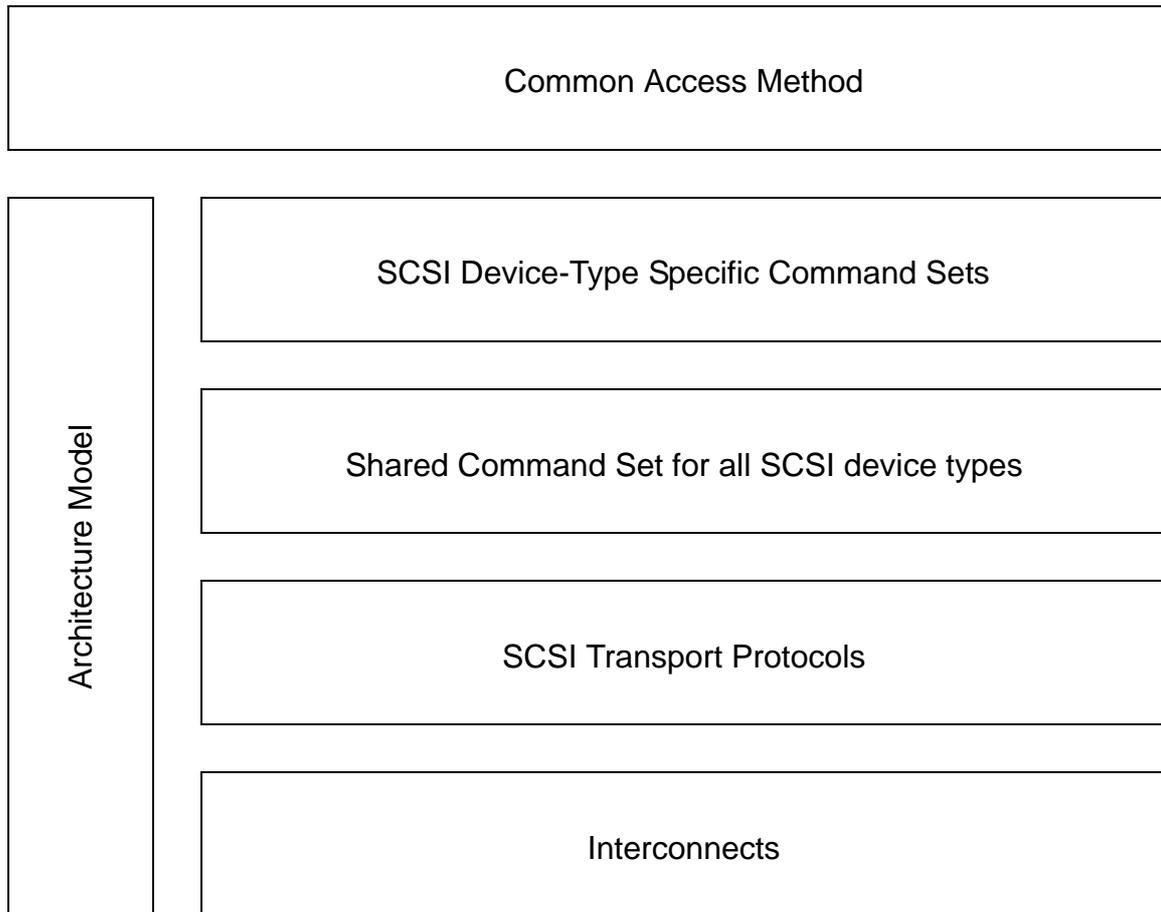


Figure 1 - SCSI Document Structure

2 Normative references

2.1 Normative references

The following referenced documents are indispensable for the application of this standard. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document, including any amendments, applies.

2.2 Approved references

IEC 60512-2:1985, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods - Part 2: General examination, electrical continuity and contact resistance tests, insulation tests and voltage stress tests*

IEC 60512-11-7:1996, *Connectors for electronic equipment - Tests and measurements - Part 11-7: Climactic tests - Test 11g: Flowing mixed gas corrosion test*

ISO 129, *Technical Drawings - Dimensioning - General principles, definitions, methods of execution and special indications*

ISO 1660, *Technical Drawings - Dimensioning and tolerancing of profiles*

2.3 References under development

At the time of publication, the following referenced standards were still under development. For information on the current status of the document, or regarding availability, contact the relevant standards body or other organization as indicated.

ISO/IEC 14776-121, *Information technology - Small Computer System Interface (SCSI) - Part 121: Passive Interconnect Performance (PIP)*

ISO/IEC 14776-313, *Information technology - Small Computer System Interface (SCSI) - Part 313: Primary Commands-3 (SPC-3)*

ISO/IEC 14776-412, *Information technology - Small Computer System Interface (SCSI) - Part 412: Architecture Model 2 (SAM-2)*

2.4 Other references

For information on the current status of the listed documents, or regarding availability, contact the indicated organization.

EIA-700AOAE (SP-3651), *Detail Specification for Trapezoidal Connectors with Non-removable Ribbon Contacts on 1.27 mm Pitch Double Row used with Single Connector Attachments (SCA-2)*

EIA-700AOAF (SP-3652), *Detail Specification for Trapezoidal Connector 0.8 mm Pitch used with Very High Density Cable Interconnect (VHDCI)*

SFF-8451, *SCA-2 Unshielded Connections*

NOTE 1 - For more information on the current status of the document, contact the SFF committee at 408-867-6630 (phone), or 408-867-2115 (fax). To obtain copies of this document, contact the SFF committee at 14426 Black Walnut Court, Saratoga, CA 95070 at 408-867-6630 (phone) or 408-741-1600 (fax).

T10/1378DT, *SCSI Domain Validation technical report*

NOTE 2 - For more information on the current status of the T10 document, contact the INCITS Secretariat at 202-737-8888 (phone), 202-638-4922 (fax) or via Email at incits@itic.org. To obtain copies of this document, contact Global Engineering at 15 Inverness Way, East Englewood, CO 80112-5704 at 303-792-2181 (phone), 800-854-7179 (phone), or 303-792-2192 (fax).